MULTI-FUNCTION RESISTANCE CHANGE MEMORY CELLS AND APPARATUSES INCLUDING THE SAME

PRIORITY APPLICATION

[0001] This application is a continuation of U.S. application Ser. No. 14/456,510, filed Aug. 11, 2014, which is a continuation of U.S. application Ser. No. 13/428,944, filed Mar. 23, 2012, now issued as U.S. Pat. No. 8,804,399, all of which are incorporated herein by reference in their entirety.

BACKGROUND

[0002] Computers and other electronic systems, for example, digital televisions, digital cameras, and cellular phones, often have one or more memory devices to store information. Increasingly, memory devices are being reduced in size to achieve a higher density of storage capacity. However, memory devices also need to meet lower power requirements while maintaining high speed access.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. **1** shows a block diagram of a memory device having a memory array with memory cells, according to an embodiment;

[0004] FIG. **2** shows a partial block diagram of a memory device having a memory array including memory cells with access components and memory elements, according to an embodiment;

[0005] FIG. **3** shows a schematic diagram of a memory cell having an access component coupled to a memory element, according to various embodiments;

[0006] FIG. **4** is a simplified schematic block diagram of one of several resistance change memory cell (RCM) memory elements that may be used with the memory devices of FIGS. **1** and **2**, or may comprise the memory cell of FIG. **3**;

[0007] FIGS. **5**A through **5**C show a schematic representation of ionic migration and localized conductive region formation and growth of a RCM;

[0008] FIG. **6** is a voltage-time graph showing a number of programming/erase pulses;

[0009] FIG. **7** shows an embodiment of a memory array circuit that may be used to implement variable resistance states and memory function types;

[0010] FIG. **8** is a flowchart showing an embodiment of a method to implement variable resistance states and memory functions; and

[0011] FIG. **9** shows a block diagram of a system embodiment, including a memory device.

DETAILED DESCRIPTION

[0012] The description that follows includes illustrative apparatuses (circuitry, devices, structures, systems, and the like) and methods (e.g., processes, protocols, sequences, techniques, and technologies) that embody the inventive subject matter. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide an understanding of various embodiments of the inventive subject matter. It will be evident, however, to those skilled in the art that various embodiments of the inventive subject matter may be practiced without these specific details. Further, well-known apparatuses and methods have not been shown in detail so as not to obscure the description of various embodiments.

[0013] As used herein, the term "or" may be construed in an inclusive or exclusive sense. Additionally, although various exemplary embodiments discussed below may primarily focus on two-state (e.g., SLC) memory devices, the embodiments are merely given for clarity of disclosure, and thus, are not limited to apparatuses in the form of SLC memory devices or even to memory devices in general. As an introduction to the subject, a few embodiments will be described briefly and generally in the following paragraphs, and then a more detailed description, with reference to the figures, will ensue.

[0014] Emerging memory technologies may be utilized based on the intrinsic characteristics of an advanced memory device, rather than to attempt to force the device to behave, for example, as a flash memory or random access memory. In various embodiments described herein, managing the memory operations of an advanced memory device from an abstracted interface entails novel operation schemes.

[0015] Various embodiments enable a managed memory solution that capitalizes on the characteristics of an advanced memory device. For example, a resistance change memory cell (RCM) memory device (e.g., including devices such as a programmable metallization cell) exhibits data retention characteristics that depend on the amplitude and time duration of a signal pulse (e.g., a voltage or current signal). As will become apparent, differentiated memory function types may be managed on a single chip. In some embodiments, all electrical routing is within a single chip, so that through-silicon vias (TSVs) and critical alignment between adjacent chips are no longer required. In addition, latency may be reduced on a single chip implementation, as compared with fabricating a system over multiple chips.

[0016] In various embodiments, an apparatus is provided that includes a number of resistance change memory (RCM) cells. The apparatus includes a first region of the RCM cells, a second region of the RCM cells, and drive circuitry to selectively provide one of a plurality of signal pulse types to the first region of the RCM cells and to selectively provide a different one of the plurality of signal pulse types to the second region of the RCM cells. Each of the plurality of signal pulse types have a different attribute and corresponding to a different memory function type

[0017] In at least some of embodiments of the apparatus, the attribute comprises an integration of a pulse amplitude and a pulse time duration.

[0018] In various embodiments, an apparatus is provided that includes a number of memory regions; each of the memory regions having a respective number of resistance change memory cells. A control and select circuitry is to determine a memory function type to emulate for information to be stored in the apparatus. The control and select circuitry further to select one of the memory regions in which to store the information. Drive circuitry is to provide to the selected one of the memory regions a pulse configured to emulate the determined memory function type for the information.

[0019] In some embodiments of the apparatus, the memory regions, the control and select circuitry, and the drive circuitry are all formed on a single die. In some embodiments of the apparatus, the drive circuitry is to provide a pulse having an amplitude and time duration